AF

PTO/SB/21 (09-06)
Approved for use through 03/31/2007. OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission

Application Number	09/933,492
Filing Date	08-20-2001
First Named Inventor	DAVID R. HEMBREE
Art Unit	2815
Examiner Name	CHU, CHRIS
Attorney Docket Number	00-0625.01

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
- [x] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):
  Return receipt postcard

Remarks

Enclosed is an Appeal Brief in response to the rejections in the Final Office Action dated 10-10-2006.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	LAW OFFICE OF STEPHEN A. GRATTON		
Signature			
Printed name	Stephen A. Gratton		
Date	01-10-2007	Reg. No.	28,418

CERTIFICATE OF TRANSMISSION/MAILING

I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:

Signature			
Typed or printed name	Stephen A. Gratton	Date	01-10-2007

PTO/SB/17 (07-06)
Approved for use through 01/31/2007. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2006

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application Number	09/933,492
Filing Date	08-20-2001
First Named Inventor	DAVID R. HEMBREE
Examiner Name	CHU, CHRIS
Art Unit	2815
Attorney Docket No.	00-0625.01

METHOD OF PAYMENT (check all that apply)

☒ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 07-1857 Deposit Account Name: Stephen A. Gratton

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 (including Reissues)	50	25
Each independent claim over 3 (including Reissues)	200	100
Multiple dependent claims	360	180

Total Claims _____ - 20 or HP = _____ x _____ = _____ Extra Claims / Fee ($) / Fee Paid ($)

HP = highest number of total claims paid for, if greater than 20.

Indep. Claims _____ - 3 or HP = _____ x _____ = _____ Extra Claims / Fee ($) / Fee Paid ($)

HP = highest number of independent claims paid for, if greater than 3.

Multiple Dependent Claims Fee ($) _____ Fee Paid ($) _____

3. APPLICATION SIZE FEE

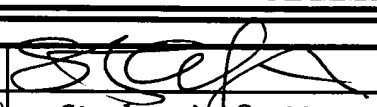
If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets _____ - 100 = _____ Extra Sheets / 50 = _____ Number of each additional 50 or fraction thereof (round up to a whole number) x _____ Fee ($) = _____ Fee Paid ($)

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other (e.g., late filing surcharge): Appeal Brief	500.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 28,418	Telephone 303 989 6353
Name (Print/Type)	Stephen A. Gratton		Date 01-10-2007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

David R. Hembree
Alan G. Wood

Serial No.: 09/933,492 Art Unit: 2815

Filing Date: 08/20/2001

For: SEMICONDUCTOR COMPONENT HAVING CONDUCTORS WITH DIGITAL DATA PATTERN (AS AMENDED)

Examiner: Chu, Chris

Attorney Docket No. 00-0625.1

APPEAL BRIEF

January 10, 2007

Mail Stop Appeal Brief - Patents
Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

This Appeal Brief is being filed concurrently with the Notice of Appeal mailed on 01/10/2007, in response to the rejections contained in the final Office Action mailed 10/10/2006.

Also being submitted is the $500 fee under 37 CFR 41.20(b)(2) for the Appeal Brief.

TABLE OF CONTENTS

(Claim 8, appealed)

8. A system for converting existing TV content to an interactive TV program according to Claim 4, wherein the remote control unit is modified to transmit a series of directional button presses to the set top box, and the interactive TV utility program detects the remote control signals and causes an on-screen cursor in a fixed reference point in the display area to aim in corresponding directional increments and illuminate a vector ray at a target hot spot position in the display area.

(Claim 9, appealed)

9. A system for converting existing TV content to an interactive TV program according to Claim 8, wherein the reference point is a whimsical object appearing in a fixed position in the display area and the vector ray is a part or action of the whimsical object sent to a target hot spot position.

(Claims 10-12, withdrawn)

(Claim 13, canceled)

(Claim 14, appealed)

14. A method for converting existing TV content to an interactive TV program according to Claim 16, wherein the hot spot positions are specified as coordinate locations in the display area.

(Claim 15, appealed)

15. A system for converting existing TV content to an interactive TV program according to Claim 16, wherein the hot spot positions are specified as marker positions in an HTML-

type "page" that is parsed or overlaid to display the hot spot positions in the display area.

(Claim 16, appealed)

16. A system for converting existing TV content to an interactive TV program comprising:

(a) providing TV content in the form of a series of successive display frames in a time sequence;

(b) providing object mapping data specifying display locations of objects as hot spots positions appearing in the display frames of the TV content to be rendered interactive;

(c) operating an interactive TV utility program in a TV set top box to process linkages from objects specified by the object mapping data to respective interactive functions to be performed upon viewer selection of the objects in conjunction with a display of the TV content; and

(d) operating a TV display system including the TV set-top box and associated remote control unit to display the TV content and use the object mapping data to determine when the viewer is pointing to and selecting an object appearing in a display frame with the remote control unit and cause the interactive function linked by the corresponding linkage of the interactive TV utility program to be performed, and further comprising adapting the remote control unit with directional buttons and a selecting button as a pointing device.

i. REAL PARTY IN INTEREST

The real party in interest in the appeal is Micron Technology Inc., the assignee of record of the patent application.

ii. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this appeal.

iii. STATUS OF CLAIMS

Claims 1-51 (canceled).

Claims 52-62 (rejected).

Claims 63-69 (canceled).

Claims 70-77 (rejected).

Claims 52-62 and 70-77 are being appealed.

iv. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the final Office Action mailed 10/10/2006.

v. SUMMARY OF CLAIMED SUBJECT MATTER

The rejected claims are directed to a semiconductor component (un-numbered) which is shown in Figures 4. The component includes a substrate 10 (Figure 4, page 7, line 9) comprising a plurality of semiconductor components 12 (Figure 4, page 7, line 10). As described on page 7, lines 8-23 of the specification, the substrate 10 (Figure 4) can comprise a semiconductor wafer, and the semiconductor components 12 (Figure 4) can comprise semiconductor dice 54 (Figure 7B) or semiconductor packages 52 (Figure 7B).

Each semiconductor component 12 (Figure 4) includes a plurality of component contacts 28 (Figure 4, page 7, line 21), such as bond pads 58 (Figure 7B, page 16, line 21), and a plurality of integrated circuits 56 (Figure 7B, page 16, lines 20-22) in electrical communication with the component contacts 28 (Figure 4). In addition, the semiconductor components 12 (Figure 4) include a plurality of good components (same as semiconductor components 12-Figure 4), and at least one defective component 12D (Figure 4). The good components 12 and the defective component 12D are initially described on page 7, lines 24-30 of the specification.

Each component 12 (Figure 4) also includes a plurality of redistribution conductors 22 (Figure 2F, page 14, lines 10-13) configured to perform the functions of redistributing the component contacts 28 (Figure 4) on the good components 12 (page 10, lines 22-30), and of either repairing, reconfiguring, or electrically isolating the defective components 12D (page 13, line 22 to page 14, line 9). In addition, the conductors 22 (Figure 2F) have a pattern containing information (page 13, lines 27-29) in

the form of digital data 36 (Figure 3) representing the locations of the good components 12, the defective component 12D and the component contacts 28 (page 12, lines 8-15).

vi. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. Whether the drawings show the feature of "the conductors having a pattern containing information from testing of the semiconductor component".

2. Whether the limitation in the claims of "the conductors having a pattern containing information from testing of the semiconductor components" represents new matter introduced into the disclosure.

3. Whether claims 52, 56, 60 and 70 fail to satisfy the written description requirement of 35 USC §112, first paragraph because the limitation "the conductors having a pattern containing information from testing of the semiconductor components" is not supported by the specification.

4. Whether claims 52-62 and 70-77 are indefinite under 35 USC §112, second paragraph, due to the limitations of:

(a) "a plurality of redistribution conductors... in electrical communication with the component contacts configured to repair the defective component";

(b) "the conductors having a pattern containing information from testing of the semiconductor components.... for repairing the defective component".

5. Whether claims 52-62 and 70-77 are anticipated under 35 USC §102(e) by Tanizawa (US Patent No. 4,721,995).

vii. ARGUMENT

1. Objection to the drawings

The objection to the drawings is based on the recitation in the claims of "the conductors having a pattern containing information from testing of the semiconductor component".

However, the conductors 22 are shown in Figures 2F and 2J. In addition, conductors 22P in a singulated component 52 are shown in Figure 7B. Further, Figure 4 illustrates how defective components 12D can be electrically isolated by the conductors 22. Figure 5 illustrates how defective components 12D can be excluded from clusters C11, C2, C3, C4 by the conductors 22. Figure 7B illustrated how the conductors 22P function to redistribute the pattern of component contacts (bond pads 58) to the pattern of terminal contacts 64.

Still further, verbatim antecedent basis for the "information" characteristics of the conductors is provided on page 13, lines 27-29 of the specification. Verbatim antecedent basis for the "pattern" characteristic of the conductors is provided on page 5, line 6; page 10, line 20; page 11, line 1; page 12, lines 3 and 30; page 13, line 23; and page 14, line 11 of the specification.

With regard to the examiner's interpretation of 37 CFR 1.83(a), it is submitted to be incorrect. Although the drawings must show every feature of the invention specified in the claims, all the characteristics of the feature do not need to be shown in the drawings. For example, if the Applicant were to claim the conductors as having a "high conductivity", or a "reflective surface", these characteristics would not need to be shown in the drawings. Similarly, the presently claimed characteristic of the

conductors "having a pattern containing information" need not be shown in the drawings, because it is explained in the specification.

In this regard, under MPEP 608.02, drawings are required "where necessary for the understanding of the subject matter to be patented". In the present case, the drawings show details of the conductors including structure, method of fabrication and function. In addition, the specification goes into even greater detail on the structure, method of fabrication and function of the conductors. In view of the originally filed drawings and specification, it is submitted that one skilled in the art would understand the claimed subject matter.

Accordingly, the objection to the drawings is submitted to be in error.

2. Objection to new matter introduced into the disclosure

The new matter objection is based on the limitation "the conductors having a pattern containing information from testing of the semiconductor components ".

In regard to this limitation, please note page 13, line 22, to page 14, line 9, of the specification.

"Referring again to Figure 1, the redistribution layer 20 can be etched with the conductors 22 in *patterns* selected to achieve different objectives. As a first example, the redistribution layer 20 can be etched to repair or re-configure defective components 12D (Figures 4 and 5). Specifically, the initial testing step identifies the defective components 12D and *this information is contained in the digital data 36 (Figure 3)* supplied to the modulator 34. Some defects can be corrected by providing

conductors 22 that substitute redundant circuitry contained on the defective components 12D for defective circuitry.

Other defects can be corrected by configuring or re configuring the component 12D in a particular electrical format. For example, a memory component (e.g., DRAM) may be defective when configured as a 1 Meg X 16 device (i.e., 1 megabit deep by 16 bits wide = 16 megabits of total memory). However, the memory component may not be defective when configured as a 4 Meg X 4 device (i.e., 4 megabits deep by 4 bits wide = 16 megabits of total memory). *By electrically connecting, or alternately electrically isolating, selected component contacts 28 using the conductors 22 different configurations can be achieved.*" (italics added)

In view of the foregoing original disclosure, the new matter objection is submitted to be in error.

3. 35 USC §112, second paragraph, rejections of claims 52, 56, 60 and 70 due to insufficient written description

The 35 USC §112, second paragraph, rejections of claims 52, 56, 60 and 70 due to insufficient written description are submitted to be in error. With regard to these rejections the final Office Action states:

"In claims 52, 56, 60 and 70 the specification fails to describe the phrase "the conductors having a pattern containing information from testing of the semiconductor components".

As argued above, the specification supports the above limitation in the passage at page 13, line 22 to page 14, line 9 quoted in the previous section on new matter.

With regard to these rejections, the final Office Action further states:

"The final product of the invention clearly shows in Fig. 2J, Fig. 7, Fig. 7A, Fig. 7B and page 12, line 1-page 13, line 32 that the conductors 22p or 22 are just normal wiring circuits which are formed by etching the redistribution layer 30 according to the data received from the digital data 36."

Appellant disagrees that one skilled in the art would interpret the conductors 22p or 22 as just normal wiring circuits. Rather, the conductors have a physical structure that is different than conventional wiring on a semiconductor wafer. Specifically, the conductors have a unique pattern containing information from testing the semiconductor components. This information allows the conductors to perform the additional functions of either repairing, reconfiguring, electrically isolating the defective component, or clustering of the good components.

In view of the disclosure supporting the above recitation, the insufficient written description rejection is submitted to be in error.

4. 35 USC §112, second paragraph, rejections of claims 52, 56, 60 and 70 due to indefiniteness

The 35 USC §112, second paragraph, rejections of claims 52, 56, 60 and 70 due to indefiniteness are submitted to be in error. With regard to these rejections the final Office Action states:

(a) Regarding the limitation "a plurality of redistribution conductors . . . in electrical communication with the component contacts configured to repair the defective components" how is the plurality of conductors configured to repair the defective component?".

For an explanation, the specification and drawings of the application must be read and understood. Claims are to be read in light of the specification. In re Okuzawa, 537 F.2d 563, 190 USPQ 464 (CCPA 1976). In addition, only a person of ordinary skill in the art to which the invention pertains need be enabled by the application disclosure. In re Naquin, 158 USPQ 317 (CCPA 1968).

Accordingly, the present disclosure is directed to artisans of ordinary skill in semiconductor packaging. In this regard, "redistribution conductors" are well known to those skilled in the art of semiconductor manufacture.

As stated on page 10, lines 22-30 of the specification:

"In addition, the conductors 22 can be configured to locate or "fan out" terminal contacts (e.g., solder balls) for the components 12 in a desired pattern, such as a dense grid array. Redistribution layers are well known in the art of semiconductor manufacture for configuring different types of components."

From the above disclosure, one skilled in the art would know that the conductors 22 are configured to perform a redistribution function. However, as an additional function, the conductors 22 are configured to either repair, reconfigure, electrically isolate or exclude the defective components 12D from clusters.

With regard to the indefiniteness rejections, the final Office Action further states:

(b) Regarding the limitation "the conductor having a pattern containing information from testing of the semiconductor components... for repairing the defective component" it is unclear how the pattern of a conductor contains information from testing of the semiconductor

components . . . when the conductor is nothing more than a metal wire and not software".

However, a map is nothing more than lines on a piece of paper, but it contains information. A book is nothing more than an assembly of words, but it contains information. In the present case, the conductors comprise metal lines on a substrate, but they contain information in the form of a unique pattern that allows defective components to be repaired, reconfigured, electrically isolated or excluded from clusters.

Appellant would further respond that in formulating claims, an applicant may use either conventional terms, or may be his own lexicographer, as long as the meaning is clear. In re Cataing, 429 F.2d 461, 166 USPQ 550 (CCPA 1970).

In the present case, the pattern of conductors includes information in the form of digital data. This information provides the conductors with a physical structure that performs the function of repairing, reconfiguring, electrically isolating or excluding the defective components 12D from clusters. It is submitted that when read in light of the specification this meaning is clear, and that the metes and bounds of the claims can be ascertained. Accordingly, the indefinite rejections are submitted to be in error.

5. 35 USC §102(e) rejections of claims 52-62 and 70-77 over Tanizawa

The rejections under 35 USC §102(b) are traversed because this reference does not disclose or enable all of the limitations of the claimed semiconductor component. A first limitation not discloses or enabled by Tanizawa is

"redistribution conductors having a pattern containing information from testing of the semiconductor components".

In Tanizawa an insulative film 5 (Figures 3(a), 3(b)) includes two types of circuit patterns 6 (column 3, lines 14-16). The circuit patterns 6 are the conductive traces which are shown in Figure 3(a) without a reference numeral. As shown in Figures 3(a) and 3(b), and described at column 3, lines 14-33, the first type of circuit patterns 6 are used to interconnect good circuit blocks 2. As shown in Figures 6(a) and 6(b), and described at column 3, lines 35-54, the second type of circuit patterns 6 are used to connect repair chips 8, which are stacked on and bonded to defective circuit blocks 2 (column 6,lines 21-23).

The circuit patterns 6 in Tanizawa are not "redistribution conductors on the components" as presently claimed, but rather are wiring patterns on a separate film which interconnect the components. In this regard, please note Figure 3(a) of Tanizawa wherein the circuit blocks 2 (components in the present claims) include component contacts (pads 4-Figure 3(b)). However, as shown in Figure 3(a), the circuit patterns 6 are not on the circuit blocks 2, but rather are in the streets between the circuit blocks 2. Also, the circuit patterns do not function as "redistribution conductors" because they do not redistribute the pattern of the component contacts (pads 4-Figure 3(b)), but rather interconnect the circuit blocks 2.

Redistribution conductors have a special purpose in the art (see page 10, lines 25-30 of the present specification), which is not performed by the circuit patterns 6 in Tanizawa. At the time of the Tanizawa patent (10/05/1984) redistribution conductors were not utilized.

The circuit patterns 6 in Tanizawa cannot and do not perform the function of redistribution conductors.

In addition to not being redistribution conductors, the circuit patterns 6 do not have a pattern containing information from testing of the ICs as presently claimed, but rather have a universal pattern that allows any circuit block 2 (Figure 4) identified as being defective to be replaced by a repair chip 8 (Figure 6b).

In the rejections, the examiner has characterized the recitation of the "conductors having a pattern containing information from testing of the semiconductor components...for repairing the defective component" as being "functional or intended use language that does not differentiate the claimed structure over Tanizawa".

However, the examiner's interpretation of this claim language is incorrect. The subject recitation is neither functional nor intended use language. Functional language means a structure is stated to perform a certain function, which is not the case here. Intended use language means a structure can be used for a certain purpose, which is also not the case here. Rather, the presently claimed conductors, are stated to have the physical characteristic of a pattern containing information from testing of the components. This physical characteristic allows the conductors to perform the stated functions of repair, reconfiguration, electrical isolation, or connection of good components in clusters.

As the recitation is submitted to be structural rather than functional, it is submitted to distinguish the claimed component from the art. Also please note that under the criteria established by MPEP 2114, and In re Schreiber, 128 F.3d 1473, 1477-78, 44 USPQ 1429, 1431-2 (Fed Cir. 1997),

the above noted structural limitation distinguishes the claimed component from the prior art.

MPEP 2114 also states: "A prior art device can perform all the functions of the apparatus claims and still not anticipate the claim. Even if the prior art device performs all the functions recited in the claim, the prior art cannot anticipate the claim if there is any structural difference."

In support of the rejections, the examiner also states "Since the term "information" is defined as the locations (i.e., the good components, the defective component and the component contacts) and the patterned conductor of Tanizawa also represents the locations (i.e., the good components, the defective component and the component contacts), the patterned conductor of Tanizawa contains the information. Thus Tanizawa meets the claim."

This interpretation of the claims and the reference is submitted to be incorrect. In the present component, the conductors not only locate the good components and the defective component, but they also either repair the defective component, reconfigure the component contacts, electrically isolate the defective component, or connect good components in clusters. In Tanizawa, the defective circuit block 2 (defective component) is electrically isolated by punching out the circuit pattern 6 corresponding to the defective circuit block 2 (column 3, lines 19-21). The defective circuit block 2 is then replaced by a repair chip 8 (Figure 6b).

With respect to the rejections under 35 USC §102, each independent claim includes a different recitation on the configuration of the redistribution conductors.

Accordingly, each independent claim is being argued separately.

Independent claim 52 and dependent claims 53-55

Independent claim 52 recites "redistribution conductors on the components .... having a pattern containing information from testing of the semiconductor components representing locations of the good components, the defective component and the component contacts, and for repairing the defective component".

The feature of redistribution conductors configured to perform a repair function is not disclosed or enabled by Tanizawa. In this regard, the circuit patterns 6 (Figure 3(a)) in Tanizawa are not "redistribution conductors" on the circuit blocks 2 (Figure 3(a)), but rather are traces on an insulative film 5, which are located between the circuit blocks 2.

Although the defective circuit blocks 2 in Tanizawa are "replaced" they are not "repaired". With respect to the repair function of the presently claimed "redistribution conductors" page 13, line 24 to page 14, line 1 of the present specification states:

"As a first example, the redistribution layer 20 can be etched to repair or re-configure defective components 12D (Figures 4 and 5). Specifically, the initial testing step identifies the defective components 12D and this information is contained in the digital data 36 (Figure 3) supplied to the modulator 34. Some defects can be corrected by providing conductors 22 that substitute redundant circuitry contained on the defective components 12D for defective circuitry.

Other defects can be corrected by configuring or re configuring the component 12D in a particular electrical format."

As redistribution conductors configured to perform a repair function are not disclosed or enabled by Tanizawa, the 35 USC §102 rejections of claims 52-55 are submitted to be in error.

Independent claim 56 and dependent claims 57-59

Independent claim 56 recites "redistribution conductors on the components configured to electrically isolate the component contacts on the defective component, the conductors having a pattern containing information from testing of the components representing locations of the good components, the defective component and the component contacts, and for electrically isolating the defective component."

Admittedly the circuit patterns 6 in Tanizawa are configured to electrically isolate defective circuit blocks 2. However, the circuit patterns are not "redistribution conductors" on the components as presently claimed, but rather are traces on an insulative film 5 located between the circuit blocks 2.

As redistribution conductors configured to perform an isolation function are not disclosed or enabled by Tanizawa, the 35 USC §102 rejections of claims 56-59 are submitted to be in error.

Independent claim 60 and dependent claims 61-62

Independent claim 60 recites "redistribution conductors on the components having a pattern containing information from testing of the semiconductor components

representing locations of the good components, the defective component and the component contacts, the conductors configured to reconfigure the component contacts on the defective component."

The circuit patterns 6 in Tanizawa are not configured to reconfigure the pads 4 on defective circuit blocks 2. Rather the circuit patterns 6 are punched out to electrically isolate defective circuit blocks 2 (column 3, lines 19-21).

With respect to the "reconfigure" limitation, the Office Action states: "Since the contacts 4 on the bad chip 2 are physically attached to the contacts 9 on the good chip 8 thru the good chip 8 the contacts 9 read as reconfigured contact of the contacts 4. Thus Tanizawa fully meets this limitation."

However, the circuit patterns 6 are not performing a reconfiguration of the component contacts even under this interpretation of Tanizawa. Rather, the repair chip 8 is an additional element that replaces the defective circuit block 2. The previously cited passage on page 13, line 24 to page 14, line 1 of the present specification state what is meant by the term "reconfigure" in the present claims.

As redistribution conductors configured to reconfigure component contacts are not disclosed or enabled by Tanizawa, the 35 USC §102 rejections of claims 60-62 are submitted to be in error.

Independent claim 70 and dependent claims 71-77

Independent claim 70 recites "a metal redistribution layer on the substrate comprising a plurality of redistribution conductors having a pattern containing information from testing of the semiconductor components

representing locations of the good components, the defective component and the component contacts, the conductors configured to either repair, reconfigure, or electrically isolate the defective component, or to electrically connect multiple good components in a cluster that excludes the defective component."

The circuit patterns 6 in Tanizawa are not a metal redistribution layer on a substrate. In addition, the circuit patterns 6 in Tanizawa do not inherently perform the function of a metal redistribution layer. Further, the circuit patterns 6 in Tanizawa are not configured to either repair a defective component, reconfigure component contacts on a defective component, electrically isolate a defective component or cluster good components.

As a redistribution layer and redistribution conductors configured to perform the stated functions are not disclosed or enabled by Tanizawa, the 35 USC §102 rejections of claims 70-77 are submitted to be in error.

viii. Claims appendix

52. A semiconductor component comprising:

a substrate comprising a plurality of semiconductor components, each component including a plurality of component contacts and a plurality of integrated circuits in electrical communication with the component contacts, the components including a plurality of good components and at least one defective component; and

a plurality of redistribution conductors on the components in electrical communication with the component contacts configured to repair the defective component, the conductors having a pattern containing information from testing of the semiconductor components representing locations of the good components, the defective component and the component contacts, and for repairing the defective component.

53. The component of claim 52 wherein the components include a second defective component and the conductors are configured to electrically isolate the second defective component.

54. The component of claim 52 wherein the components include a second defective component and the conductors are

configured to reconfigure the component contacts on the second defective component.

55. The component of claim 52 wherein the components include a second defective component and the conductors are configured to electrically connect multiple components in a cluster that excludes the second defective component.

56. A semiconductor component comprising:

a substrate comprising a plurality of components including a plurality of component contacts;

the components including a plurality of good components and at least one defective component; and

a plurality of redistribution conductors on the components configured to electrically isolate the component contacts on the defective component, the conductors having a pattern containing information from testing of the components representing locations of the good components, the defective component and the component contacts, and for electrically isolating the defective component.

57. The component of claim 56 further comprising a plurality of terminal contacts on the good components in

electrical communication with the conductors and the component contacts on the good components.

58. The component of claim 56 wherein the conductors are configured to electrically connect a plurality of good components in a cluster that excludes the defective component.

59. The component of claim 56 wherein the substrate comprises a semiconductor wafer, and the components comprise semiconductor dice or semiconductor packages.

60. A semiconductor component comprising:

a substrate comprising a plurality of semiconductor components, each component comprising a plurality of integrated circuits and a plurality of component contacts in electrical communication with the integrated circuits, the components including a plurality of good components and at least one defective component; and

a plurality of redistribution conductors on the components having a pattern containing information from testing of the semiconductor components representing locations of the good components, the defective component and the component contacts, the conductors configured to

reconfigure the component contacts on the defective component.

61. The component of claim 60 further comprising a plurality of terminal contacts on the good components in electrical communication with the conductors and the component contacts on the good components.

62. The component of claim 60 wherein the substrate comprises a semiconductor wafer or portion thereof and the components comprise dice or packages.

Claims 63-69 (canceled)

70. A semiconductor component comprising:

a substrate comprising a plurality of semiconductor components including a plurality of good components and at least one defective component, each component comprising a plurality of component contacts and a plurality of integrated circuits in electrical communication with the component contacts; and

a metal redistribution layer on the substrate comprising a plurality of redistribution conductors having a pattern containing information from testing of the

semiconductor components representing locations of the good components, the defective component and the component contacts, the conductors configured to either repair, reconfigure, or electrically isolate the defective component, or to electrically connect multiple good components in a cluster that excludes the defective component.

71. The component of claim 70 wherein the good components include a plurality of terminal contacts in electrical communication with the component contacts on the good components.

72. The component of claim 70 wherein the component contacts comprise bond pads.

73. The component of claim 70 wherein the conductors on the good components have a fan out configuration.

74. The component of claim 70 wherein the substrate comprises a semiconductor wafer.

75. The component of claim 70 further comprising a protective layer on the conductors on the good components.

76. The component of claim 70 wherein the components comprise semiconductor packages or dice.

77. The component of claim 70 wherein the components include a second defective component and the conductors are configured to repair, reconfigure or electrically isolate the second defective component.

ix. Evidence appendix

Included are copies of the evidence relied upon by the examiner as to the grounds of rejection under 35 USC §102 to be reviewed on appeal.

1. Tanizawa (US Patent No. 4,721,995)

x. Related proceedings appendix

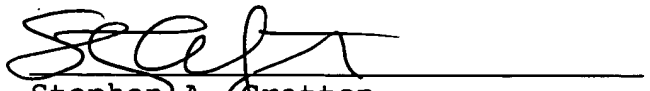
None.

Conclusion

In view of the foregoing arguments, Appellant submits the rejections of claims 52-62 and 70-77 are not proper. Appellant thus requests reversal of the rejections, and allowance of claims 52-62 and 70-77.

DATED this 10th day of January, 2007.

Respectfully submitted:



Stephen A. Gratton
Registration No. 28,418
Attorney for Appellant

2764 South Braun Way
Lakewood, CO 80228
Telephone: (303) 989 6353
Fax: (303) 989 6538

CERTIFICATE OF MAILING UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class mail in an envelope addressed to: Mail Stop Appeal Brief - Patents, Commissioner For Patents, PO BOX 1450, Alexandria, VA 22313-1450 on this 10th day of January, 2007.

01/10/2007
Date of Signature

Stephen A. Gratton, Attorney for Appellant